Semiconductor device mfg method - involves forming field oxide film for element isolation structure without deterioration of device characteristic, e.g. oxide film breakdown voltage
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Patent Family

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Patent Details

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JP 8097203	A		4	H01L-021/316	

Abstract:
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The mfg method involves forming a pad oxide film (2) on surface of a Si substrate (1). A polysilicon film (3) is then formed on the pad oxide film at 624 deg.C.

A Si3N4 film is formed on polysilicon film and has a thickness of 100-180 nm. A resist is applied on Si3N4 film and patterning is performed to develop a resist pattern (5). A field oxide film(6) is formed to obtain an element isolation structure by performing field oxidation at 1050 deg.C.

ADVANTAGE - Eases element isolation and stress committed to edge part of active region. Prevents deterioration in device. Improves breakdown voltage.

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